ZERO BIAS GaInAs MISFET MIXERS

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Abstract

This paper reports the experimental results of a passive, switch-type single-ended mixer using a metal-insulator-semiconductor field effect transistor (MISFET) that was fabricated from $Ga_{0.47}In_{0.53}As$ (GaInAs). The device operated without any applied DC drain or gate bias. A third order input intercept point as high as +30 dBm was obtained with +20 dBm LO input power. Also presented are harmonic balance simulations of the mixer circuit.

Introduction

Maas[1] has recently demonstrated that the dynamic range of a narrow-band passive single-ended mixer, using a GaAs MESFET, compares favorably with the double-balanced diode mixer. Furthermore, the MESFET requires much lower LO power. Weiner *et al*[2] have also used the passive-mode MESFETs in a double-balanced mixer configuration to achieve similar dynamic range performance over multi-octave bandwidth. However, a negative gate bias is essential for the GaAs MESFET mixer to avoid gate forward conduction. Generally speaking, an ideal FET for this type of mixer should have very linear channel on/off impedances, very rapid transition between the on/off states, and high input power handling capability[3].

GaInAs's high electron mobility and peak velocity make the material preferable to other semiconductors at room temperature. Because of its low barrier height (-0.3V), a MISFET structure is preferred for the GaInAs devices. In fact, the MISFET structure can operate with zero gate DC bias, allows equal positive and negative gate-voltage swings, and provides a wider range of nearly constant transconductance. Therefore, the GaInAs MISFET[4] (Figure 1) has a desirable combination of characteristics for the operation of passive, switch-type FET mixers.

The present work will show that similar or better mixer performances of the passive, gate-biased GaAs MESFET mixers are achievable using the GaInAs MISFET with no gate bias. Therefore, the MISFET mixer has the advantage of circuit simplification, especially when the single-ended mixers are utilized to realize the double-balanced mixers for further performance improvement.

To assist in the design of the mixer circuit, harmonic balance simulations of the circuit were performed using the program NANA[5]. The simulations made use of the GaAs MESFET model developed by Curtice and Ettenberg[6] to account for variations of drain-source current as the device's state is modulated by the LO and RF signals. The multiple signal input capabilities of NANA enable the observation of higher order effects, such as intermodulation products.

Mixer Design

In a passive FET mixer, the FET device is operated in its linear, ohmic region where no drain DC bias voltage is applied to the FET. The FET device is essentially treated as an RF switch with its on/off states determined by the FET channel impedance, which in turn is controlled by the LO signal applied directly to the gate. The reported mixer is in principle similar to the passive silicon metal-oxide-semiconductor (MOS) FET mixer, which has the highest reported dynamic range in the VHF frequency range[7]. More details regarding passive FET mixer designs can be found in references 1, 2, and 7.

A simplified equivalent circuit of the GaInAs MISFET, along with the single-ended mixer circuit, is shown in Figure 2(a). A photograph showing the complete mixer in a test fixture is given in Figure 2(b). The GaInAs MISFET mixer has circuit topology similar to that employed in reference 1, i.e., a two-section coupled-line bandpass filter for RF port and a low-high impedance line low-pass filter for IF port. The LO circuit is simply a 50-ohm microstrip line with tuning pads along the line. This type of an LO

circuit readily supports impedance matching for different devices. Note that no DC bias is applied to the MISFET gate. The MISFET mixer was physically realized on a 25-mil alumina substrate with a dielectric constant of 9.8.

Device Fabrication

The hydride synthesis VPE technique (In, Ga, AsH_3, and HCl) was applied to grow GaInAs epilayers that were lattice-matched to SI InP substrates for depletion-mode (normally-on) MISFETs. The MISFETs were fabricated using a self-aligned-gate (SAG) process to minimize gate overlap capacitances, while providing a full-gate MISFET structure (this process is essential for good device stability). The doping density profile of a typical wafer, measured on an electrochemical profiler, is shown in Figure 3. These MISFETs have excellent DC characteristics, with transconductances (g_m) as high as 280 mS/mm gate width. Gate lengths were ~0.7 μm, and the gate oxide thickness was estimated to be 55 nm. These values give a calculated cutoff frequency $f_t = g_m/2\pi C_g$ of about 100 GHz.

Experimental Results

RF conversion loss and intermodulation of the mixer were measured using an HP-8566 spectrum analyzer. Figure 4 shows the measured mixer RF bandwidth for an available LO power of 13 dBm. The minimum conversion loss measured 6.2 dB, including the 0.7 dB RF filter loss. The bandwidth was limited primarily by the RF filter response. This minimum conversion loss can be further reduced by using a device having a shorter gate length, such as a FET with a gate length of 0.3 μm (see Table 1).

Figure 5 shows the measured two-tone third-order input intercept point as a function of LO power, with RF frequencies near 11 GHz. The RF input power was -7 dBm for each RF tone. A third-order input intercept point as high as +30 dBm has been obtained for the MISFET single-ended mixer. The LO power required to achieve the high intercept point may be reduced by better input matching at the LO port (VSWR at the LO port was greater than 2.6 in the present case). Note that the MISFET structure is able to handle more than +20 dBm input power without any negative gate bias.

Table 1 summarizes the experimental results of an X-band single-ended passive depletion-mode GaInAs MISFET mixer. Data for diode and other GaAs MESFET mixers are shown for comparison.

Computer Simulation

The harmonic balance program NANA (for *N*on-linear *ANA*lysis) was used to help predict the conversion loss of the mixer circuit described above. The simulation of the circuit required careful modeling of the MISFET device and its surrounding passive components in the circuit.

To model the device, DC I-V data were obtained using a Hewlett-Packard 4145 semiconductor analyzer. The Curtice-Ettenberg model was fitted to the data by adjusting the parameters A_0, A_1, A_2, A_3, β, and γ in the following equations:

$$I_{ds} = (A_o + A_1V_1 + A_2 V_1^2 + A_3V_1^3) \cdot \tanh(\gamma V_{out}(t))$$

with:

$$V_1 = V_{in}(t-\tau)\cdot[1 + \beta(V^\circ - V_{out}(t))]$$

V_{in} and V_{out} represent the gate-to-source and drain-to-source voltages, respectively; I_{ds} is the drain current. Note that the constant term V° (nominally 4 V for power amplifiers) has been set to zero to improve the fit of the model at the low drain and gate voltages of the circuit. Although the model was originally intended for FETs in power amplifier circuits, Figure 6 shows that the model also fits the MISFET data reasonably well. The intrinsic gate resistance, gate-drain, gate-source, and drain-source capacitances of the device were obtained by fitting a conventional small-signal model of the FET to zero-bias S-parameter data. We have assumed that these capacitances do not change significantly as the device is turned on and off.

All passive structures in the circuit (including microstrip and coupled lines) were first simulated using Super Compact to provide for NANA the effective Y-matrices of the linear subnetworks making up the circuit. During the NANA simulations, an LO of 8 GHz and an RF input tone of 11.0 GHz were applied to the circuit. Assuming up to third order intermodulation, the harmonic balance procedure accounted for the presence of fundamental, IF, intermodulation, and harmonic components at 3, 5, 8, 11, 14, 16, 19, and 22 GHz. Components beyond 22 GHz were assumed insignificant and therefore not accounted for.

The simulations predicted a conversion loss of 8.2 dB at an RF input of 11 GHz. This compares favorably to a measured value of 8.6 dB (see Figure 4). Figure 7 shows the simulated power spectrum at the mixer's IF port. The near zero operating conditions of the circuit imposed numerical instabilities for the harmonic balance algorithms. This problem has precluded a two-tone intermodulation simulation of the circuit, and deserves further investigation.

Conclusions

The experimental and computer simulation results of an X-band passive single-ended mixer using GaInAs MISFETs have been reported. The experimental data has shown that a third order input intercept point as high as +30 dBm can be achieved without any gate or drain bias. Further performance improvement should be achievable using smaller GaInAs MISFET devices in a balanced mixer configuration. Computer simulations using the NANA program have been successfully applied to predict the conversion loss of the mixer. Further efforts in the device modeling and computer algorithms are required to accurately predict the intermodulation distortion performance of a passive mixer with multiple input signals.

Acknowledgements

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References

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TABLE 1. Spur-free dynamic range (SFDR)

Mixer Type	CG	NF	IP_3	P_{LO}	SFDR
D.B. Diode	-7.5	7.5	18	10	76
D.D.B. Diode	-7.5	7.5	25	21	81
Active MESFET AT 10650	6.0	5.0	10	10	73
Passive MESFET NEC 673	-6.0	6.0	27	10	83
Passive HEMT JS 8902	-7.0	7.0	27	10	83
Passive MISFET DSRC R899	-8.1	8.1	20	13	77
	-7.0	7.0	30	20	85
	-6.8	6.8	33	23	87

NOTES:
SFDR calculated at a bandwidth of 10 MHz; CG = conversion gain; NF = noise figure; IP_3 = calculated input third order intercept point.

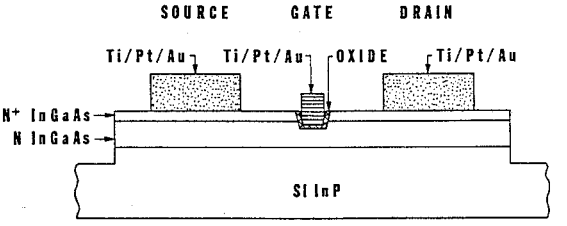

Figure 1. Schematic cross-section of self-aligned-gate GaInAs MISFET structure.

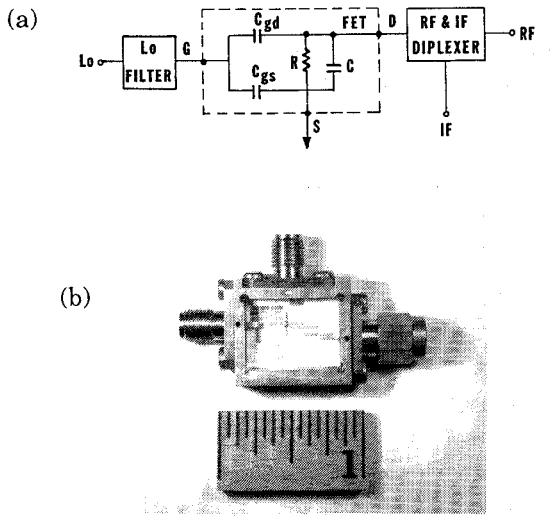

Figure 2. Single-ended mixer. (a) Circuit diagram; (b) Photo of circuit.

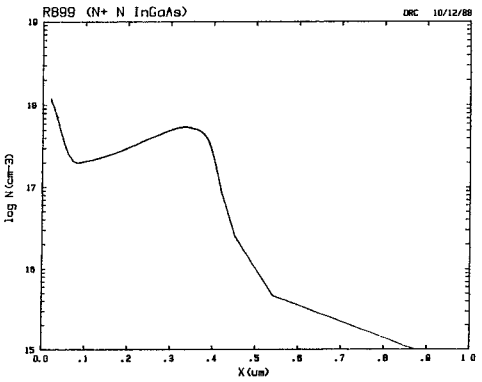

Figure 3. Typical n+-n- GaInAs/Si InP doping density profile obtained in VPE reactor.

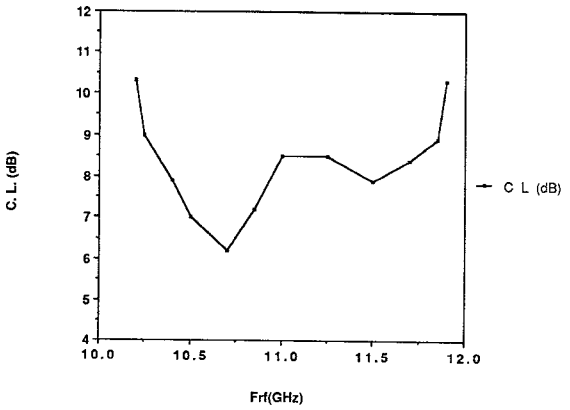

Figure 4. Conversion loss as a function of RF frequency. Available LO power is 13 dBm at 8 GHz.

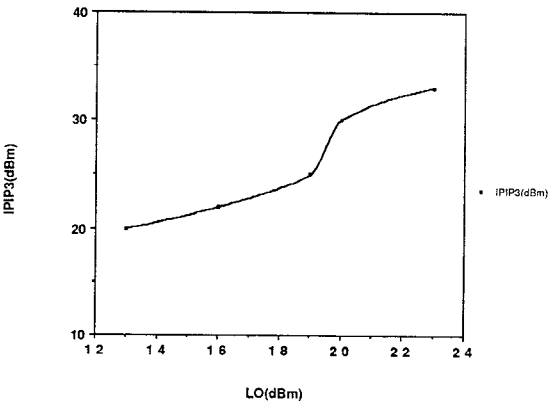

Figure 5. Measured third-order input intercept point as a function of LO power level. Each RF tone has an available input power of -7 dBm.

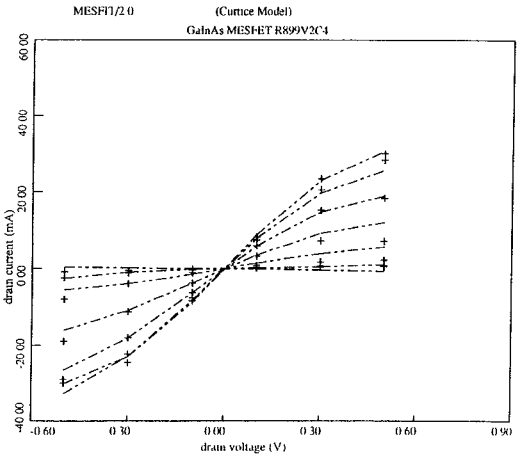

Figure 6. Normal operating region of a passive FET mixer and DC curve fitting.

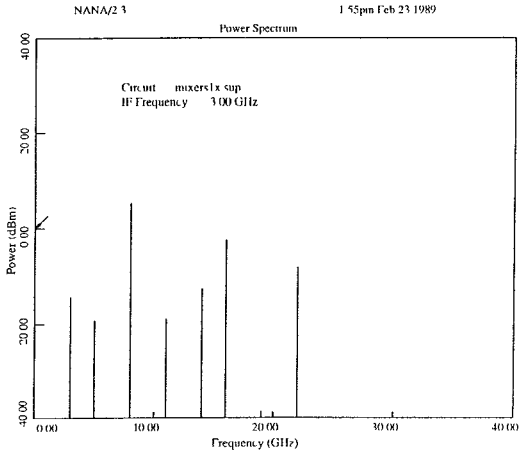

Figure 7. Simulated power spectrum at the mixer IF output.